UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/533,042	03/22/2000	Ryuichi Sunayama	826.1597/JDH	7804

21171 7590 01/24/2003

STAAS & HALSEY LLP
700 11TH STREET, NW
SUITE 500
WASHINGTON, DC 20001

EXAMINER
KNAPP, JUSTIN R

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 01/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/533,042	Applicant(s) SUNAYAMA ET AL.
	Examiner Justin Knapp	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/22/00, 8/8/00* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Papers Submitted

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Foreign Priority document as received 03/22/00, Information Disclosure Statement as received 03/22/00, and Change of Address/Power of Attorney as received 08/08/00.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Losq, "Subroutine Return Address Stack", IBM Technical Disclosure Bulletin, December 1981.

5. Referring to claims 1 and 16, Losq has taught:

a) a storing circuit storing information specifying a return address of a subroutine when an instruction equivalent to a subroutine call is detected. On page 1, lines 26-27 and page 2, lines 1-8, Losq has taught a storing circuit consisting of a Branch History Table and Subroutine Return

Address Stack storing information specifying a return address of a subroutine when a call is detected.

b) a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in said storing circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected. On page 2, lines 40-46, Losq has taught a decoder used as comparing circuitry to compare R1 of a BALR or similar instruction on the return stack, which holds information specifying the return address, and R2 of a BCR or similar instruction which holds the branch destination address of a potential subroutine return instruction.

c) an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison. It is inherent in the system disclosed by Losq, that identifying circuitry must be present since Losq's system is able to identify an instruction equivalent to a subroutine return.

6. Referring to claim 2, Losq has not explicitly taught a storing circuit which stores a register number of a link register, which is specified by the instruction equivalent to the subroutine call, as the information specifying the return address. However, it is inherent the return address stack (storing circuit) stores a register number of a link register specified by a BALR instruction (potentially an instruction equivalent to a subroutine call) due to the format of a BALR instruction (see IBM ESA/390 Principles of Operation, pages 7-14 – 7-15).

7. Referring to claim 3, Losq has taught said storing circuit stores the return address of the subroutine as the information specifying the return address (See page 1, lines 24-27 and page 2, lines 1-13).

8. Referring to claims 4 and 17, Losq has taught:

a) a stack circuit storing information specifying a return address of a subroutine (See page 1, lines 25-27 and page 2, lines 1-4).

b) a push circuit pushing the information specifying the return address onto said stack circuit, when an instruction equivalent to a subroutine call is detected (Page 1, lines 26-27 and page 2, lines 1-2 inherently show push circuitry exists to push information specifying a return address down onto the stack).

c) a comparing circuit making a comparison between information specifying a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return and the information specifying the return address stored in a top entry of said stack circuit, and outputting a result of a comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected. As explained herein above, this is inherent.

d) an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison. As explained herein above, this is inherent.

9. Referring to claim 5, Losq has taught:

a) said push circuit pushes a register number of a link register, which is specified by the instruction equivalent to the subroutine call, onto said stack circuit as the information specifying the return address. As explained herein above, this is inherent.

b) said comparing circuit makes a comparison between a register number of a branch destination address register, which is specified by the instruction which can possibly be the instruction equivalent to the subroutine return, and a register number stored in the top entry of said stack circuit. As explained herein above, this is inherent.

c) said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return when the compared register numbers match. As explained herein above, this is inherent.

10. Referring to claim 6, Losq has taught said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return regardless of the result of the comparison, if the register number of the branch destination address register corresponds to a particular register. Losq has taught that if a potential equivalent to a subroutine return corresponds to a particular register (see page 2, lines 2-8).

11. Referring to claim 7, Losq has taught said push circuit does not push the register number of the link register onto said stack circuit if the register number of the link register corresponds to a particular register. If the R2 field of BALR instruction corresponds to a particular register, 0, nothing is pushed onto the stack (ESA/390 Principles of Operation, page 7-15, Programming notes: 2.).

12. Referring to claim 8, Losq has taught a pop circuit popping said stack circuit when said identifying circuit identifies the instruction which can possibly be the instruction equivalent to the subroutine return as the instruction equivalent to the subroutine return, and a branch by the

instruction equivalent to the subroutine return is taken (see page 2, lines 44-46 show that pop circuitry in the system of Losq is inherent).

13. Referring to claim 9, Losq has taught:

a) a predicting circuit storing branch history information for a branch prediction (Losq's system contains a branch history table in it's predicting circuitry to store branch history information), wherein

b) said comparing circuit makes the comparison between the information specifying the branch destination address and the information specifying the return address, when the branch history information is registered to said predicting circuit. A comparing circuit is inherent as explained herein above including when the branch history information is registered in the branch history table to said predicting circuit.

14. Referring to claim 10, Losq has taught a circuit invalidating the information stored in said storing circuit when an event which causes correspondence between a subroutine call and a subroutine return to be improper. A circuit invalidating information stored in said storing circuit is inherent since the return address stack is not popped when there is a improper correspondence between a subroutine call and return (see page 2, lines 44-47 and page 3, line 1).

15. Referring to claim 11, Losq has taught:

a) a predicting circuit storing branch history information for a branch prediction (as taught herein above);

b) a setting circuit setting in said predicting circuit a flag indicating that a return destination of a detected instruction equivalent to a subroutine return differs, when an instruction equivalent to a subroutine return, which does not return to an instruction address immediately succeeding the

instruction equivalent to the subroutine call, is detected. It is inherent the predicting circuit of Losq must use some type of flag to indicate that a return destination of potential subroutine return differs or the system would not function correctly.

16. Referring to claim 12, it is inherent the system disclosed by Losq has said predicting circuit comprises a return address stack circuit storing the return address of the subroutine, pops said return address stack circuit if the flag is recognized at the time of a branch prediction, and does not use a popped return address as a predicted branch destination. It is necessary to be able to pop a return address on a return address stack if a return address has to be removed but not used.

17. Referring to claim 13, Losq has taught:

a) predicting circuit storing branch history information for a branch prediction (as explained herein above);

b) a circuit performing a control such that a predetermined flag is set when an instruction equivalent to a subroutine call, which is unregistered to said predicting circuit, is detected, the predetermined flag is reset when an instruction equivalent to a subroutine return, which corresponds to the unregistered instruction equivalent to the subroutine call, is detected, and the instruction equivalent to the subroutine return corresponding to the unregistered instruction is not identified as an instruction equivalent to a subroutine return is said predicting circuit. It is inherent the system disclosed by Losq must be able to handle instruction equivalent to a subroutine calls not registered to said predicting circuit.

18. Referring to claims 14 and 18, Losq has taught

a) a return address stack circuit storing a return address of a subroutine when an instruction equivalent to a subroutine call is detected (see page 1, lines 24-26);

b) a comparing circuit making a comparison between a branch destination address of an instruction which can possibly be an instruction equivalent to a subroutine return, and the return address stored in said return address stack circuit, and outputting a result of the comparison, when the instruction which can possibly be the instruction equivalent to the subroutine return is detected. This is inherent as explained herein above.

c) an identifying circuit identifying an instruction equivalent to a subroutine return, which corresponds to the instruction equivalent to the subroutine call, based on the result of the comparison. This is inherent as explained herein above.

19. Referring to claim 15, the method in claim 15 does not recite limitations above the claimed device set forth in the above claims and is therefore rejected for the same reasons set forth in the rejection of the above claims.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin Knapp whose telephone number is (703) 308-6132. The examiner can normally be reached on Mon - Fri 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Justin Knapp
Examiner
Art Unit 2183

January 23, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100